APPLICATION

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TITLE: VERTICALLY-STACKED CO-PLANAR TRANSMISSION LINE STRUCTURE FOR IC DESIGN

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A VERTICALLY-STACKED CO-PLANAR TRANSMISSION LINE STRUCTURE FOR IC DESIGN

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates generally to a vertically-stacked co-planar transmission line structure for an IC (integrated circuit) design, and more particularly pertains to on-chip transmission line designs that have superior loss and reflection characteristics relative to conventional on-chip transmission line designs.

2. Discussion of the Prior Art

[0002] Conventional on-chip transmission lines are routed in a single metal layer in an IC chip's metal-dielectric stack which result in inferior loss and reflection characteristics.

[0003] Stacked conductors have been used in prior art on-chip spiral stacked inductor designs. In these designs, the lower resistance of the stacked conductors results in higher Qs (quality factors) for the spiral inductors.

[0004] During operation of prior art on-chip spiral stacked inductors, most of the current flowing in the conductors is located against the inside edges (edges closest to the center of the spiral inductor). Therefore, by increasing the cross sectional area of the conductors at the inside edges of the inductor lines, the resistance in the lines is reduced, thus increasing the Q value achievable by the inductor.

[0005] However, the prior art on-chip spiral stacked inductor lines are quite different in implementation and purpose from the stacked coplanar micro-strip/waveguides of the present invention, and are not transmission lines in the sense of being a waveguide interconnect structure having two or more conductors and defining a closed ground return path within the waveguide interconnect structure.

SUMMARY OF THE INVENTION

[0006] Accordingly, the present invention provides a vertically stacked co-planar transmission line structure for an IC design, wherein a transmission line is defined as a waveguide interconnect structure having two or more conductors and defining a closed ground return path within the waveguide interconnect structure.

[0007] The transmission line designs of the present invention comprise metal lines in multiple metal and via levels in the metal-dielectric stack of an IC chip. A simple structure metal transmission line comprises a metal layer, the next metal layer down, and the via metal interposed between the two metal layers, all with equal width and length dimensions.

[0008] The on-chip stacked coplanar micro-strip/waveguides of the present invention allow chip designers to design a much wider range of characteristic impedances, and also provide dramatic improvements in insertion loss and reflection loss to low-impedance source and load terminations. The structure is designed to be used for long sensitive on-chip interconnects, provides superior performance over conventional one-metal layer structures, and allows custom engineering of the transmission line characteristic impedance.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] The foregoing objects and advantages of the present invention for a vertically-stacked co-planar transmission line structure for an IC design may be more readily understood by one skilled in the art with reference being had to the following detailed description of several embodiments thereof, taken in conjunction with the accompanying drawings wherein like elements are designated by identical reference numerals throughout the several views, and in which:

[0010] Figure 1 is a vertical cross sectional view of an on-chip coplanar micro-strip structure comprising a pair of first and second coplanar stacked conductors, each comprising a metal layer, the next metal layer down, and a wide via bar in between the two metal layers in the upper metal layers of an RF/BiCMOS technology.

[0011] Figure 2 shows a similar type of on-chip coplanar micro-strip structure comprising a pair of first and second coplanar stacked conductors implemented in a typical base CMOS8SF technology.

[0012] Figures 3(a) through 3(d) illustrate four different on-chip stacked coplanar transmission line (micro-strip/waveguide) configurations in the base CMOS8SF technology: a) Differential +, - pair; b) Coplanar Signal,Ground micro-strip; c) Ground,Signal,Ground; d) Ground, +, -, Ground.

[0013] Figure 4 illustrates an embodiment which adds an additional via bar and metal layer onto the bottom of the coplanar micro-strip/waveguide in Figure 1, making the conductor in this type of embodiment three metal layers and two via layers tall.

[0014] Figure 5 illustrates the results of a simulation comparison and illustrates graphs of S-parameter results in the base CMOS8SF technology for an ideal stacked coplanar micro-strip line, a design rule limited stacked coplanar micro-strip line, and a conventional coplanar micro-strip line.

[0015] Figure 6 illustrate the results of a simulation comparison and illustrates graphs of R, L, C, and Z(f) results in CMOS8SF technology for an ideal stacked coplanar micro-strip line, a design rule limited stacked coplanar micro-strip line, and a conventional coplanar micro-strip line.

DETAILED DESCRIPTION OF THE INVENTION

[0016] The present invention provides new on-chip transmission line designs that have superior loss and reflection characteristics relative to conventional on-chip transmission line approaches. In the context of the present invention, a transmission line is defined as a waveguide interconnect structure having two or more conductors and defining a closed ground return path within the waveguide interconnect structure.

[0017] Conventional on-chip transmission lines are routed in a single metal layer in the chip's metal-dielectric stack. In contrast thereto, the transmission line design of the

present invention consists of metal lines in multiple metal and via levels in the chip's metal-dielectric stack. The simplest structure is a metal transmission line that is comprised of a metal layer, the next metal layer down, and the via metal in between the two metal layers (all with equal width and length dimensions). This structure can either be a coplanar differential pair of conductors as shown in Figure 3(a) or a coplanar micro-strip as shown in Figure 3(b).

[0018] Figures 1 and 2 illustrate two exemplary embodiments of coplanar micro-strip lines comprised of first and second coplanar stacked conductors.

[0019] Figure 1 is a vertical cross sectional view of an on-chip coplanar micro-strip structure comprising a pair of first and second coplanar stacked conductors 10, 12, each comprising a metal layer m(i), the next metal layer down m(i-1), and a wide via bar in between the two metal layers in the upper metal layers of an RF/BiCMOS technology. More specifically, each stacked conductor comprises the metal in metal layer m(i), the metal in metal layer m(i-1), and the metal in an intermediate connecting via layer marked via. Each stacked conductor has a height H and a width W (wherein the subscript s stands for signal and the subscript g stands for ground), and the stacked conductors are separated by a distance S. The height of the metal layer m(i) is hm(i), the height of the metal layer m(i-1) is hm(i-1), and the height of the intermediate connecting via layer is hvia.

[0020] Figure 2 shows a similar type of on-chip coplanar micro-strip structure comprising a pair of first and second coplanar stacked conductors 20, 22 implemented in a typical base CMOS8SF technology. Wide via bars over 0.4 μm are not permitted under the base CMOS8SF design rules, so the connecting via metal layer consists of several long parallel via bars 24 spaced 0.4 μm apart. In Figure 2, three parallel via bars 24 are provided per stacked conductor. Notice that the via bars are placed such that they are as close to the *inside* edge 26 of the stacked conductor as possible (the edge facing the other line conductor in the micro-strip pair).

[0021] Figures 3(a) through 3(d) illustrate four different on-chip stacked coplanar transmission line (micro-strip/waveguide) configurations in the base CMOS8SF technology.

[0022] Figure 3 (a) illustrates a differential +, - pair transmission line structure wherein the micro-strip pair of first and second vertically stacked coplanar conductors comprise a differential positive and negative pair of transmission line conductors labeled respectively + and -.

[0023] Figure 3(b) illustrates a coplanar signal, ground micro-strip wherein the micro-strip pair of first and second vertically stacked coplanar conductors comprise signal S and ground GND transmission line conductors.

[0024] Figure 3(c) illustrates a ground, signal, ground transmission line structure further comprising a third vertically stacked coplanar conductor wherein the first, second and third vertically stacked coplanar conductors comprise respectively ground GND, signal S and ground GND lines of a waveguide transmission line structure.

[0025] Figure 3(d) illustrates a ground, +, -, ground transmission line structure further comprising third and fourth vertically stacked coplanar conductors, wherein the first, second, third and fourth vertically stacked coplanar conductors comprise respectively a ground GND, a differential positive + and negative - pair of transmission line conductors and a ground of a waveguide transmission line structure.

[0026] By using vertical connection vias as long interconnects instead of simple vertical posts, extra thick transmission lines can be implemented. Figures 1-3 illustrate coplanar micro-strip/waveguides constructed from two metal layers m(i) and m(i-1) and the via metal between the two metal layers (via). Notice that the total height (thickness) of the coplanar micro-strips in Figures 1 and 2, H, is equal to hm(i) + hvia + h(i-1). This provides a greater capacitance per unit length than a coplanar micro-strip line of the same dimensions constructed using only m(i) or m(i-1). In fact, the height advantage is nearly a factor of three improvement in a typical base CMOS8SF metal/dielectric stack. Therefore, the characteristic impedance is lower relative to a coplanar micro-strip line with the same dimensions in either of the two individual metal layers.

[0027] By reducing the lowest possible characteristic impedance in on-chip coplanar micro-strips and waveguides, the RF IC designer is given more flexibility and control in designing transmission lines with lower reflective (S_{11},S_{22}) losses at the source and load line terminations. A major improvement is also possible in the reduction of the magnetic field extension into the lossy silicon substrate by confining EM energy more compactly between the thicker metal line edges of the coplanar micro-strip/waveguide structures depicted in Figures 1-2. DC resistance (as well as AC resistance) can be greatly reduced for the structures shown in Figures 1-3 over conventional single metal layer coplanar micro-strip/waveguide structures. The lower resistance of these conductors can also be used to combat DC losses in power and ground supply lines in high-density VLSI CMOS as well as reducing charge and discharge times in long high-speed digital lines.

[0028] The on-chip stacked coplanar micro-strip/waveguides allow a design of a much wider range of characteristic impedances to chip designers as well as dramatic improvements in insertion loss and reflection loss to low-impedance source and load terminations. The structure is designed to be used for long sensitive on-chip interconnects. It provides superior performance over conventional one-metal layer structures as well as allowing custom engineering of the transmission line characteristic impedance.

[0029] In the stacked coplanar micro-strip cross section shown in Figure 2, the current is concentrated at the edges 26 of the micro-strip conductors that are nearest to the neighboring line. Via bars located at this edge have a similar effect on the line resistance of the long straight coplanar micro-strip as on a prior art on-chip spiral inductor as described above. However, in addition to decreasing resistance, when used in a coplanar micro-strip/waveguide structure, the increase in height H due to metal-via-metal stacking can be used to custom engineer the characteristic impedance of the coplanar micro-strip/waveguide. As mentioned before, the characteristic impedance achievable with the stacked transmission line configurations depicted in Figure 3 are lower than any similar conventional configurations possible in the present state of the art.

[0030] Figure 4 illustrates an embodiment which adds an additional via bar labeled via 2 and an additional metal layer (mi-2) onto the bottom of the coplanar micro-

strip/waveguide in Figure 1, making the conductor in this type of embodiment three metal layers and two via layers tall. The three metal layers comprise a metal layer m(i), a next metal layer down m(i-1), and a second next metal layer down m(i-2), and a first intermediate connecting via layer labeled via 1 in between the metal layer and the next metal layer down, and a second intermediate connecting via layer labeled via 2 in between the next metal layer and the second next metal layer down.

[0031] Similar types of five layer embodiments could be implemented with respect to the embodiments of Figures 2 and 3, and additional seven or more layer embodiments could be implemented with respect to the embodiments of Figures 1, 2 and 3.

[0032] The coplanar micro-strip/waveguide structures shown in Figures 1, 2 can be implemented in existing IBM technologies such as BiCMOS7WL and CMOS8SFG. The ideal stacked coplanar micro-strip structure is shown in Figure 1, where a via bar with the same width as the lines of metal above and below is possible. Unfortunately, lithography and etch bias based design rules do not permit this in most technologies as any misalignment in metal levels will cause increased resistance . In CMOS8SFG, via bars (0.4 um wide) at VQ level need to be at least 0.55 um within above-lying LM line level. In 7WL, via bars (1.24 um wide) at FT level need to be at least 1 um within above-lying E1 line level.

[0033] From a fabrication standpoint, analog vias of thickness up to 4 um have been demonstrated in SiGe technologies like 5DM, 7HP, 7WL etc. Precedent exists for the routing of long via bars in the form of the stacked inductors enabled in 7WL and 8SF and the long bar vias routinely used in chip crack-stop guard rings. The maximum length of any allowable VQBAR in CMOS8SFG is 320 um. However, there are examples when this limit is exceeded such as spiral inductors and crack-stop guard rings. In a recent 7HP testsite, via bars for a stacked inductor, with a total running length of 765 um, have been demonstrated with no via RIE process modifications. Conventional metal deposition and planarization processes can be exercised to generate structurally reliable via bars similar to ground-rule square vias.

[0034] Another process restriction on such bar vias is that the allowable density in a 63x63 um2 area should not exceed 12%. While designing vertical coplanar

micro-strip/waveguide structures, this limitation would have to be addressed since exceeding the via area will cause the resist/ARC to be too thin.

[0035] In CMOS8SFG, bar vias are permitted at VQ level only for inductors and as part of the chip-guard. This is primarily to prevent continuous monitoring of non-POR sized vias to check etch/lithography tolerances in a manufacturing technology. Via bars of the size permitted in the stacked inductors can be applied without any modification to the vertical coplanar micro-strip/waveguide structures. The use of longer bar vias (>320 um) into a manufacturable process has also been demonstrated with the results from the recent 7HP testsite.

[0036] Electromagnetic modeling of the coplanar micro-strip structures shown in Figure 1-2 was performed using Ansoft's high-frequency structure simulator (HFSS) 7.0. The lines in the coplanar micro-strip were simulated by assigning even and odd mode ports to the differential line pair. The coplanar micro-strip structures were modeled for both the base CMOS8SF and BiCMOSWL technologies. In the base CMOS 8sf technology, the following dimensions (from Figure 2) were assigned to the stacked coplanar micro-strip structure: W_S=W_G=5 μm, S=2 μm, H=1.85 μm, hm(i)=0.6 μm, hm(i-1)=0.6 μm. The total micro-strip length was 1mm, representing a long on-chip interconnect line. The long parallel via bars in between metal layer m(i) and m(i-1) were each 0.4 μm wide and spaced 0.4 μm apart. All metal and via layer heights as well as via widths and spacing were taken from the CMOS8SF design manual. For the simulations, a five metal layer process was assumed in the CMOS8SF technology such that m(i) is the LM metal layer and m(i-1) is the MQ metal layer and the via bar exists in the VQ via layer.

[0037] Figures 5 and 6 illustrate the results of a simulation in which a stacked coplanar micro-strip structure was compared to a conventional coplanar micro-strip. The conventional micro-strip was assigned exactly the same dimensions, but existed in only the top metal layer (or m(i)/LM).

[0038] The traces 50 represent the simulation results for the ideal stacked coplanar micro-strip structure in the five metal layer base CMOS8SF technology. This ideal stacked

coplanar micro-strip/waveguide has a via bar whose width is equal to that of the metal lines above and below. The ideal structure cannot be fabricated with the current CMOS8SF process, but represents the performance attainable if the process were dual damascene. The traces 52 are the results for the stacked micro-strip whose cross section is currently possible in the CMOS8SF technology (same as cross section shown in Figure 2). Finally, the traces 54 are the simulation results for the same size conventional coplanar micro-strip line in only the top metal layer of the five metal layer CMOS8SF technology.

[0039] Clearly the new structure represented by the traces 52 has far superior matching to the 50 Ω source and load resistances used in the simulation (S_{11} graph in the top left corner of Figure 5). This is because the stacked structure, as predicted, has a much lower characteristic impedance than the conventional coplanar micro-strip line (Z(f) graph in the bottom right corner of Figure 6). In fact, the stacked coplanar micro-strip line shows about a 7dB improvement in matching at 500 MHz. This equates to a 55% reduction in reflective loss over the conventional coplanar micro-strip line. The total electrical loss produced in the stacked coplanar micro-strip line represented by trace 52 is approximately 0.6 dB less than that of the conventional coplanar micro-strip line at 500 MHz (or a 48% reduction). The resistance of the stacked coplanar micro-strip line (trace 52 in the resistance graph in the upper left corner of Figure 5 shows a 57% reduction at 500 MHz when compared to the conventional coplanar micro-strip trace 54.

[0040] Figure 5 illustrates the results of the simulation comparison and illustrates graphs of S-parameter results in the base CMOS8SF technology for an ideal stacked coplanar micro-strip line represented by traces 50, a design rule limited stacked coplanar micro-strip line represented by traces 52, and a conventional coplanar micro-strip line represented by traces 54.

[0041] Figure 6 illustrate the results of the simulation comparison and illustrates graphs of R, L, C, and Z(f) results in CMOS8SF technology for an ideal stacked coplanar micro-strip line represented by traces 50, a design rule limited stacked coplanar micro-strip line represented by traces 52, and a conventional coplanar micro-strip line represented by traces 54.

[0042] One outstanding benefit to the stacked coplanar micro-strip/waveguide structures of the present invention is the additional range in characteristic impedance made possible by increasing the height of the waveguide conductors. In the characteristic impedance, Z(f), results in the bottom right graph of Figure 6, the effect of this increase in height can be seen on the characteristic impedance of the stacked differential pair CPW. Note that this change has nothing to do with the decrease in resistance in the line, but is an effect of the change in the coplanar micro-strip's inductance and capacitance. It is clear from the Z(f) graph in the bottom right of Figure 6 that the stacked coplanar micro-strip line of the present invention is able to achieve dramatically lower characteristic impedances relative to a conventional coplanar micro-strip line. In fact the stacked coplanar micro-strip line shows a 53% reduction in characteristic impedance over the conventional coplanar micro-strip line at 500 MHz.

[0043] While several embodiments and variations of the present invention for a vertically-stacked co-planar transmission line structure for an IC design are described in detail herein, it should be apparent that the disclosures and teachings of the present invention will suggest many alternative designs to those skilled in the art.